REMARKS

This responds to the Office Action dated on September 13, 2007.

Claim 5 is amended, no claims are canceled, and no claims are added; as a result, claims 1-3, 5-22, 24, 25, 35-39 and 41-45 are now pending in this application.

Appellant's invention comprises in various example embodiments a variety of methods, devices, systems and machine-readable medium for maintaining coherence of cache lines in a multi-cache system.

Independent claim 1, for example, recites a method comprising:

receiving in an Ingrained Sharing Directory Cache (ISDC) an incoming operation request including an associated incoming memory address (*see* Fig. 8, block 802; p. 17, lines 3-8);

determining if the incoming operation request is an Ingrained Sharing Directory Storage (ISDS) data reply (*see* Fig. 8, block 804; p. 17, lines 9-13), wherein the ISDS data reply includes an indication of system caches sharing a memory line having the same memory address as the incoming memory address (see Fig. 3 & 9 (block 918); p. 11, lines 12-16 and p. 21, lines 13-18), wherein the indication is extracted from two or more ISDS entries matching the incoming memory address (*see* Figs. 3 & 4; p. 11, lines 12-16 and p. 13, lines 18-21);

completing a pending ISDC entry if the incoming operation request is an ISDS data reply, wherein completing includes locating a pending ISDC operation associated with the ISDS data reply in an ISDC pending request queue (see Fig. 8, blocks 808 & 810; p. 17, line 19 through p. 18, line 7);

if the incoming operation request is not an ISDS data reply and if there is an ISDC entry associated with the incoming operation request, performing the incoming operation request (see Fig. 8, blocks 804, 806 810 & 812; p. 18, lines 8-12); and

if the incoming operation request is not an ISDS data reply and if there is no ISDC entry associated with the incoming operation request, creating an ISDC entry (see Fig. 8, blocks 814-822; p. 18, line 13 through p. 19, line 13), wherein creating includes:

requesting information associated with the incoming memory address from the ISDS (see Fig. 8, block 814; p. 18, lines 13-17);

evicting another ISDC entry if there is no free ISDC entry (see Fig. 8, blocks 818; p. 19, lines 1-4), wherein evicting includes:

requesting the ISDS to store the information for the evicted ISDC entry (see Fig. 8, block 820 & Fig. 9; p. 19, lines 5-8), wherein requesting includes transferring to the ISDS bit-vector information associated with the evicted ISDC entry (see Fig. 9, block 908; p. 20, lines 11-13), wherein the bit-vector information is used by the ISDS to select two or more ISDS cells (see Fig. 9, block 908; p. 20, lines 14-15), wherein each of the two or more ISDS cells maintains a dynamic full map of shared memory lines cached in a given set of one of the system caches and has an ISDS entry to be used to store status information for the evicted ISDC entry (see Figs. 3 & 4; p. 12, line 9 through p. 13, line 23); and

designating the evicted ISDC entry to the incoming operation request (see Fig. 8, block 822; p. 19, lines 9-13);

marking the created ISDC entry as pending, wherein pending indicates that the ISDC entry is waiting to receive a data reply from the ISDS (see Fig. 8, block 822; p. 19, lines 9-13); and

storing the incoming operation request into the ISDC pending request queue(see Fig. 8, block 822; p. 19, lines 9-13).

Dependent claim 6, for example, recites "information about copies of a given memory line resides in only one of the coherence buffers" (see Fig. 3; p. 12, line 9 through p. 13, line 4).

Dependent claim 8, for example, recites "the ISDC set and the ISDS set combined include all copies of memory lines cached at any point in time in the system caches" (see p. 12, lines 3-8).

Claim Objections

Claim 5 was objected to due to informality. Applicant has amended claim 5 to overcome this objection.

§112 Rejection of the Claims

Claims 1-2, 18-21 and 35-38 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office Action states:

> Claims 1, 18 and 35 recites the limitation "where the indication is extracted from two or more ISDS entries matching the incoming memory address" in lines 6-7, 11-12 and 12-13 respectively. The limitation is not true in all conditions, such as only one cache is caching the requested data or none of the caches has the data (in this condition only one entry matches or no entry matches), thus the limitation "two or more entry matching" renders the claim indefinite. (Due to ambiguities describe[d] above the limitation is interpreted as "the indication is extracted from any number of matching entries" (i.e., none, one or more etc.).

Applicant respectfully submits that although the limitation is not true in all conditions, it is true in a number of conditions and it does describe the system being claimed. Furthermore, the limitation is fully supported from the Specification. As noted at p. 10, line 23 through p. 11, line 2 of the Specification, Applicant teaches "the evicted ISDC entry is stored in the ISDS 204 into possibly more than one entry that can be retrieved later if this memory line becomes active again." Reconsideration is respectfully requested.

§101 Rejection of the Claims

Claims 35-39, 41 and 42 were rejected under 35 U.S.C. § 101, because claims are not limited to tangible embodiments.

The Specification has been amended to clarify the description. Reconsideration is respectfully requested.

§103 Rejection of the Claims

1) The Applicable Law

As discussed in *KSR International Co. v. Teleflex Inc. et al.* (U.S. 2007), the determination of obviousness under 35 U.S.C. § 103 is a legal conclusion based on factual evidence. See *Princeton Biochemicals, Inc. v. Beckman Coulter, Inc.*, 411 F.3d 1332, 1336-37 (Fed.Cir. 2005). The legal conclusion, that a claim is obvious within § 103(a), depends on at least four underlying factual issues set forth in *Graham v. John Deere Co. of Kansas City*, 383

U.S. 1, 17, 86 S.Ct. 684, 15 L.Ed.2d 545 (1966): (1) the scope and content of the prior art; (2) differences between the prior art and the claim at issue; (3) the level of ordinary skill in the pertinent art; and (4) evaluation of any relevant secondary considerations.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Additionally, there must be a rational underpinning grounded in evidence to support the legal conclusion of obviousness. See *In re Kahn*, 78 USPQ2d 1329 (Fed. Cir. 2006), which states that, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn* citing *In re Lee*, 61 USPQ2d 1430 (Fed. Cir.2002). Additionally, "mere identification in the prior art of each element is insufficient to defeat the patentability of the combined subject matter as a whole." *In re Kahn.*

A showing of "teaching, suggestion, or motivation" to combine the prior art to meet the claimed subject matter could provide a helpful insight in determining whether the claimed subject matter is obvious under 35 U.S.C. § 103(a). *KSR International Co.*, p. 14, line 24 through p. 15, line 8. The court in KSR made it clear, however, that the "teaching, suggestion, or motivation" (TSM) test is only one tool that can be used to determine obviousness, noting that the Examiner or court simply has to "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* p. 14, lines 5-17. The court in KSR further noted that "to facilitate review, this analysis [supporting a rejection under 35 U.S.C. § 103(a)] should be made explicit." *Id.*

Specifically, the Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *See KSR Int'l Co.*, p. 14,

citing *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006); *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).

Even if adding an element to a prior art was obvious, that does not establish that the claimed invention encompasses obvious subject matter. *KSR Int'l. Co.*, p. 19, ¶ 1. Instead, following factors can still be considered to determine whether a claimed invention at issue is nonobvious under 35 U.S.C. § 103(a): (1) whether the claimed invention yields more than predictable results (id. p. 12, ¶¶ 1-2); (2) whether there is technical difficulties in combining the prior arts, requiring substantial reconstruction or redesign (id. p. 19, ¶ 1); (3) whether the prior art cannot be upgraded to or teaches away from the claimed invention (id. p. 22, ¶ 2); (4) whether the prior arts have secondary factors which may 'dislodge' obviousness – "long felt and unresolved needs", "the failure of others", "commercial success" (id. p. 2, ¶ 3); and (5) whether the prior arts require elements of the invention to be read using hindsight to be relevant to the claimed invention (p. 17, ¶ 3).

Therefore, the test for obviousness under §103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir.1985). The Examiner must, as one of the inquiries pertinent to any obviousness inquiry under 35 U.S.C. §103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990). The fact that a reference teaches away from a claimed invention is highly probative that the reference would not have rendered the claimed invention obvious to one of ordinary skill in the art. *Stranco Inc. v. Atlantes Chemical Systems, Inc.*, 15 USPQ2d 1704, 1713 (Tex. 1990). When the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious. *Id.* p. 4 citing *United States v. Adams*, 383 U.S. 39, 51-51 (1966). Additionally, critical differences in the prior art must be recognized (when attempting to combine references). *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990).

In order to take into account the inferences which one skilled in the art would reasonably make, the examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time the invention was made. *M.P.E.P.* § 2141.03 (citing *Environmental Designs, Ltd. v. Union Oil Co*, 713 F.2d 693, 218 USPQ 865 (Fed. Cir. 1983), *cert. denied*, 464 U.S. 1043 (1984)).

> The examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. Knowledge of Appellants' disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. The tendency to resort to "hindsight" based upon Appellants' disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

M.P.E.P. § 2141.03.

2) Application of '103 to the Rejected Claims

Claims 1-3, 5, 7, 9-22, 24, 35-39, 41 and 43-45 were rejected under 35 USC '103(a)

Claims 1-3, 5, 7, 9-22, 24, 35-39, 41 and 43-45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Michael et al. (U.S. Publication No. 2002/0002659 A1), Joseph et al. (U.S. Patent No. 6,405,292), Carpenter et al. (U.S. Patent No. 6,266,743), Joseph et al. (U.S. Patent No. 6,338,123, hereinafter "Joseph-2") and Lilja et al. (A Superassociative Tagged Cache Coherence Directory, submitted by applicant as an IDS on February 24, 2004, with publication date of October 10, 1994). For the reasons explained below, Applicant respectfully submits that none of the cited references, alone or in combination, teach or suggest using an Ingrained Sharing Directory Storage (ISDS) as taught by Applicant and claimed in independent claims 1, 3, 7, 10, 13, 18, 22, 35 and 39.

> In particular, in support of the 103 rejection, the Office Action states, at p. 11, that:
>
> Michael, Joseph, Carpenter and Lilja fail to teach, dynamic full map of memory lines as required by claim 1. Joseph-2 teaches dynamic full map directory keeping track of state information of memory lines cached in system caches (Joseph-2, col. 2, lines 17-49). [although] Michael, Joseph, Carpenter, Lilja fail to teach a dynamic full map of memory

> lines as required by Applicant claim 1, it would have been obvious to one having ordinary skill in the art at the time of the invention to utilized dynamic full map directory as taught by Joseph-2 in the system of Michael, Joseph, Lilja and Carpenter to improve system performance with simple coherence protocol (Joseph-2, col. 2, lines 12-15). Joseph-2 teaches multi-way dynamic full map directory, which maintains state information of local lines cached in remote caches by each way for each remote cache (Joseph-2, col. 3, lines 14-60). Joseph-2 also teaches extracting bit-vector information (Joseph-2, col. 4, lines 35-55).

As quoted above, the Office Action appears to equate, for example, Joseph-2's Complete and Concise Remote (CCR) directory (Fig. 4) to Appellant's Ingrained Sharing Directory Storage (ISDS).

Applicant respectfully disagrees with the Office Action's applying Joseph-2. The Office Action's statement fails to recognize the difference in structure between Joseph-2's CCR directory and Applicant's ISDS to maintain a full map directory of presently shared lines of local memory. Under Joseph-2's approach, for example, the coherence controller of node A needs the CCR directories for not only node A but also nodes B-H. (i.e., 'shadow directories' for node B-H as shown in Fig. 4). Therefore, if there are N nodes throughout the system, Joseph-2's coherence controller for each node requires the same number of CCR directories to provide a full map directory of a local memory line cached in the system caches throughout the remote nodes. Then, if a system cache for node B has a copy of a local memory line of node A, the coherence controller of node A obtains such information using the separate shadow directory dedicated to node B. See col. 2, lines 17-49 (with an added emphasis on lines 25-26, "The coherence controller includes shadow directories, each corresponding to one of the external shared caches"); see also col. 3, lines 14-61 (with an added emphasis on lines 48-49, "Shadows directories B-H in node A's CCR directory"); see also col. 4, line 9 ("a dedicated shadow cache for each remote cache"); see also col. 4, lines 35-55 (with an added emphasis on lines 45-46, "the inventive CCR directory has n number of w-way shadows").

In contrast, as noted at p. 11, lines 13-16 of the Specification, Applicant's ISDS stores sharing information of a local memory line by hashing it into an ISDS structure. As a result, each sharer of the local memory line (i.e., each system cache having a copy) has a separate ISDS entry. Then, the Ingrained Sharing Directory Cache (ISDC) obtains such information from the ISDS data reply indication extracted from two or more associated ISDS data entries. The ISDS,

therefore, does not require separate additional shadow directories to provide a full map directory for a local memory line cached in remote system caches, in a local node or throughout multiple nodes. Instead, the location of each entry in the ISDS is used to determine which system caches (in a local node or throughout multiple nodes) have a copy of the local memory line. To accomplish this, Applicant's invention in claims 1, 3, 7, 10, 13, 18, 22, 35 and 39 claims using as ISDS having a plurality of ISDS cells and "each of the one or more ISDS cells maintains a dynamic full map of shared memory lines cached in a given set of one of the system caches and has an ISDS entry to be used to store status information for the evicted ISDC entry." Applicant is unable to find such a teaching in any of the cited references. Therefore, the current Office Action has failed to meet his burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness as required by the MPEP and *In re Fine*.

In addition, Applicant respectfully submits that none of the cited references, alone or in combination, provides a motivation or suggestion to combine Michael, Joseph, Carpenter, Lilja with Joseph-2 to derive a method for using the ISDS as taught by Applicant and claimed in independent claims 1, 3, 7, 10, 13, 18, 22, 35 and 39.

Applicant's claimed invention allocates a cell for each system cache holding a copy of a memory line. There is no need, therefore, to store bit vector information in each cell of the ISDS. Michael describes a cache directory (810) (i.e., memory directory) in which each entry is mapped into a corresponding entry for an associated system cache in a local node (*see* e.g., Fig. 8). As noted by the Examiner, however, Michael does not teach or suggest how each entry of the cache directory keeps track of a copy of a given local memory line cached in a plurality of system caches, in a local node or throughout multiple nodes. Under traditional approach, as noted at p. 1, section 1 of Lilja, "a vector of bits is used to point to the processors [and their respective system caches] with a cached copy of the block [of a local memory]."

In contrast, as discussed above, Joseph-2's coherence controlling method uses the same number of dedicated shadow directories as the number of system caches to keep track of system caches having a copy of a given local memory line. This teaches away from using a bit vector in a memory directory as disclosed by Michael, Joseph, Carpenter and Lilja. Applicant, therefore, respectfully submits that there would not have been any motivation for one having ordinary skill

in the art to combine Josehp-2 with Michael, Joseph, Carpenter and Lilja in the manner proposed by the Examiner.

Finally, Applicant respectfully submits that neither Joseph's pending buffer nor Carpenter's eviction buffer function as the ISDC pending request queue as taught by Applicant and claimed in claims 1, 7 and 10. In particular, the Office Action states, at p. 4 & 12, that:

> Joseph teaches a coherence controller with pending buffer, which is separate from the cache as applicant argues (Joseph, Figs. 1 & 2). According to Joseph, the coherence controller includes directory controller and pending buffer, the directory controller performs the lookup with respect to cached lines in the system and receives the state information of the memory line (i.e., transaction) and puts the request waiting for information (i.e., state information) into the pending buffer (Joseph, col. 3, line 40 – col. 5, line 33).

As quoted above, the Office Action appears to equate the pending buffer in Joseph or the eviction buffer in Carpenter to Applicant's ISDC pending request queue. For following reasons, however, the statement fails to recognize the difference between Applicant's ISDC pending request queue and the pending buffer in Joseph or the eviction buffer in Carpenter.

Joseph's pending buffer (250) in the Coherence Controller (160a) is separate from the Shared/Remote Cache (130a) (i.e., system cache associated with a local processor) and from the Memory Directory (150a). As further noted at Figs. 1 & 2 of Joseph, however, Joseph does not show that the Coherence Controller (160a) has a directory cache separate from the pending buffer (250) to maintain state information for the memory lines that are being used by existing transactions. Instead, as noted at Fig. 4 and col. 3, lines 27-31 of Joseph, each entry (the PBA and PBC part) of the pending buffer consists of the valid bit (460), address field (470) and status field (480). Col. 3, lines 40-65 of Joseph further describes:

> When a request message intended for a protocol engine 500 arrives at the input operation queues 230 of the coherence controller 200 (FIG. 2), it is forwarded to the protocol engine's lookup unit 510. …
>
> In the general case, the look-up unit 510 may be commanded to perform the look-up at the directory controller 520 of the node having the memory directory in order to retrieve information as to where the requested memory location is cached in the whole system. …
>
> The look-up unit is additionally commanded to perform the pending buffer look-up in the PBA 530 to determine if there are any pending (existing) transaction requests for the same address, i.e., collisions. …

> Thus, if a collision is detected [in the pending buffer (250)], the current requesting node (arriving request) may have to wait or may be directed to try later, for example.

As quoted above, although the pending buffer 250 is checked to determine whether its memory line that matches the same address as the incoming request is in a pending state, Joseph does not teach where the incoming request itself is stored when a collision is detected in the pending buffer. Likewise, as submitted in the previous Response mailed on May 21, 2007, the cited portion in Carpenter does not show that Carpenter's eviction buffer holds an incoming ISDC request itself when the requested memory line is in a pending state in a cache directory. Instead, the cited portion of Carpenter simply shows that Carpenter's eviction buffer holds the address of the memory lines that are being evicted [from a directory]. Therefore, Applicant respectfully submits that the pending buffer in Joseph functions not as a request queue but as a directory cache such as one in Michael (e.g., Fig. 8, block 800). That is, the pending buffer in Joseph simply holds state information of currently active memory lines.

In contrast, Applicant teaches, at **Figs. 2 (block 208)** & 8 (block 822) and p. 19, lines 9-10, using the ISDC pending request queue separate from the ISDC and the ISDS to store pending operations. To accomplish this, Applicant's invention claimed in claims 1, 7 and 10 recites "determining if there is an ISDC [206] entry associated with the incoming operation request," "requesting the ISDS [204] to store the information for the evicted ISDC entry" and "storing an incoming ISDC operation request into **the ISDC pending request queue [208]**." Applicant is unable to find such a teaching in any of the cited references.

For at least one of the reasons set forth above, Applicant respectfully submits that independent clams 1, 3, 7, 10, 13, 18, 22, 35 and 39 are patentable under 35 U.S.C. §103(a) over Michael in view of Joseph, Carpenter, Joseph-2 and Lilja. Reconsideration is respectfully requested.

Claims 6, 8, 25 and 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Michael et al. (U.S. Publication No. 2002/0002659A1), Joseph et al. (U.S. Patent No. 6,405,292), Carpenter et al. (U.S. Patent No. 6,266,743), Joseph et al. (U.S. Patent No. 6,338,123, hereinafter "Joseph-2") and Lilja et al (A Superassociative Tagged Cache Coherence Directory, submitted by applicant as an IDS on 2/24/2004, with publication data of October 10,

1994) as applied to claims 3, 7, 22 and 39 above and further in view of Lai (U.S. Patent No. 5,564,035).

These claims are patentable as being dependent on a patentable base claim for at least the same reason set forth above regarding the applicable independent claims. In addition, Applicant respectfully disagrees with the Office Action's applying Lai. As noted in the discussion of claims 1, 3, 7, 10, 13, 18, 22, 35 and 39, Michael, Joseph, Carpenter, Joseph-2 and Lilja describe storing information of a cached memory line into a directory cache or a memory directory. In contrast, as noted by the Examiner and at col. 3, lines 24-35 of Lai, Lai describes storing data in either a higher level cache or a lower level cache. This teaches away from Michael, Joseph, Carpenter, Joseph-2 and Lilja's storing information of a cached memory line into a directory cache or its associated memory directory. Applicant, therefore, respectfully submits that there would not have been any motivation for one having ordinary skill in the art to combine Lai with Michael, Joseph, Carpenter, Joseph-2 and Lilja in the manner proposed by the Examiner.

With regard to claims 2, 5, 9, 11, 12, 14-17, 19-21, 24, 36-38, 41 and 43-45, these claims are patentable as being dependent on a patentable base claim for at least the same reason set forth above regarding the applicable independent claims.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have equally addressed every assertion made in the Office Action, however, this does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in

support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13 day of November, 2007.

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